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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/739,087 | 12/19/2003 | Hirohisa Kawasaki | 246826US2S | 9935 |

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| EXAMINER | |
|---|---|
| NGUYEN, JOSEPH H | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2815 | |

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 10/739,087 | KAWASAKI ET AL. |
| | Examiner | Art Unit |
| | Joseph Nguyen | 2815 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *06 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *8-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/19/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Election/Restrictions*

Applicant's election of claims 1-7 in the reply filed on 4/6/05 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

### *Claim Objections*

Claim 5 is objected to because of the following informalities: --wring-- in line 4 of page 24 of the instant application should be "wiring". Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 2 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 2, it is not understood what applicant regards as "the first and second upper ends have squarish shapes" since the first and second upper ends are protruded and have slopes, and therefore cannot form squarish shapes. This is illustrated in figure 2 of the instant application.

Regarding claim 6, it is not understood what applicant regards as "side wall insulating film which is continuously formed along side faces of the first and second wiring layers across the first and second wiring layers" since if the sidewall insulating film is continuously formed along the side faces, how can the insulating film be *across* the wiring layers if it is not formed along the upper or lower surfaces of the wiring layers? As best understood, it is assumed that the sidewall insulating film is continuously formed along the side faces "across" (e.g. into the page).

***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by May (US 2003/0013298).

Regarding claim 1, May discloses on figure 3 a semiconductor device comprising a first wiring layer 14 (left portion of element 14) having a first lower end and a first upper end protruded more than the first lower end (para [0019], lines 5-6); a second wiring layer 14 (right portion of element 14) having a second lower end and a second upper end protruded more than the second lower end (para [0019], lines 56), the

second upper end facing the first upper end with the interposition of a first gap 24, and the second lower end facing the first lower end with the interposition of a second gap 26 larger than the first gap (para [0019], lines 5-6).

May teaches that element 14 is the electrically conductive layer (para [0015], line 11). Therefore, element 14 can function as wiring layer.

Regarding claim 2, as best understood, May teaches on figure 3 the first and second upper ends have squarish shapes.

Regarding claim 3, the claim language is functional language. The first and second wiring layers 14 are electrically conductive layers (para [0015], line 11) and therefore they can function as gate electrodes.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over May and further in view of figure 38 of the acknowledged prior art (APA).

Regarding claim 4, May discloses on figure 3 substantially all the structure set forth in the claimed invention except the first and second wiring layers being gate electrodes of driver transistors facing each other in adjacent cells of an SRAM of a point symmetrical type. However, applicant discloses on figure 38 the first and second wiring

layers being gate electrodes of driver transistors facing each other in adjacent cells of an SRAM of a point symmetrical type (page 2, lines 3-4). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify May by using the structure of the gate electrodes 14 of May to obtain the first and second wiring layers being gate electrodes of driver transistors facing each other in adjacent cells of an SRAM of a point symmetrical type for the purpose of utilizing the improved gate electrodes in a SRAM device.

Claims 5-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over May and further in view of Trivedi (US 2001/0045650 A1).

Regarding claim 5, May discloses on figure 3 a *substrate* 12 (para [0015], line 10) which is formed below the first and second wiring layers 14 across the first and second wiring layers. May does not teach the substrate is semiconductor and a silicide film which is formed on an upper surface of the semiconductor substrate between the first and second wiring layers, an upper surface of the first wiring layer, and a side face of the first wiring layer opposite the second wiring layer to electrically connect the first wiring layer to the semiconductor substrate. However, Trivedi teaches on figure 4 the substrate 2 is semiconductor (para [0020], line 8) and a silicide film 32 (para [0039], lines 2-3) which is formed on an upper surface of the semiconductor substrate 2 (para [0039, lines 2-3) between the first and second wiring layers 18 (para [0023], line 5), an upper surface of the first wiring layer, and a side face of the first wiring layer opposite the second wiring layer to electrically connect the first wiring layer 18 to the

semiconductor substrate 2. Note that the silicide film electrically connects the first wiring layer to the substrate via the source/drain region 8 (para [0024], line 1). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify May by having the substrate being semiconductor and a silicide film formed on an upper surface of the semiconductor substrate between the first and second wiring layers, an upper surface of the first wiring layer, and a side face of the first wiring layer opposite the second wiring layer to electrically connect the first wiring layer to the semiconductor substrate for the purpose of increasing the packing density as taught by Trivedi.

Regarding claim 6, as best understood, Trivedi teaches on figure 3 a sidewall insulating film 20 (para [0023], lines 6-7) which is continuously formed along side faces of the first and second wiring layers across the first and second wiring layers. Note that it is interpreted herein as the sidewall insulating film continuously formed along side faces of the first and second wiring layers and into the page.

Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over May and Trivedi and further in view of figure 38 of the acknowledged prior art (APA).

Regarding claim 7, May and Trivedi together disclose substantially all the structure set forth in the claimed invention except the first and second wiring layers being a gate electrode of a load transistor and a gate electrode of a transfer transistor in an SRAM of a point symmetrical type. However, applicant discloses on figure 38 the first and second wiring layers being a gate electrode of a load transistor and a gate

electrode of a transfer transistor in an SRAM of a point symmetrical type (page 2, lines 5-7). In view of such teaching, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify may and Trivedi using the structure of the gate electrodes of May and Trivedi to obtain the first and second wiring layers being a gate electrode of a load transistor and a gate electrode of a transfer transistor in an SRAM of a point symmetrical type for the purpose of utilizing the improved gate electrodes in a SRAM device.

## *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph Nguyen whose telephone number is (571) 272-1734. The examiner can normally be reached on Monday-Friday, 7:30 am- 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306 for regular communications.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JN
April 21, 2005

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER